Amendments to the Specification:

*Please amend the paragraph that bridges pages 10 and 11 as follows:*

FIG. 6 shows a partial schematic diagram of yet another aspect of the invention, features the same as those shown in FIG. 1 being represented by identical reference numerals. In this embodiment the PRNG 10 may be switched between a Fast Clock and the Regular System Clock, the outputs of each of which are connected to inputs of respective AND gates 50,52, the other inputs of the AND gates 50,52 being connected to a Ready State signal which is also used to reset the counter ~~24~~20. The outputs of the AND gates 50,52 are connected to the inputs of an OR gate 54, the output of which clocks the PRNG. The Ready State signal is also passed via an AND gate 56 to an input of a gate 58 which also receives the feedback trigger pulse signal from the output of the counter 20, causing the down counter 20 to again pre-load a new value from the PRNG 10.